SPECIFICATION AMENDMENTS

Please replace the paragraph beginning on page 2, line 15, with the following amended paragraph:

The actuation for a write and read operation for reading data into and out of an MRAM memory cell is respectively provided by word lines (WL) 1, WL spur lines 2, digit lines 3, and bit lines 5. The reference numeral 4 denotes an active region (diffusion region), 6 denotes a strap section, 7 denotes a contact between the strap section 6 and the diffusion region 4, and 8 denotes a minimally attainable cell layout (shown hatched) of [[6 F_]] $\underline{6F^2}$ (F signifies the minimum feature size and is shown in Fig. 1 by the width F of a word line 1, by way of example).

Please replace the paragraph beginning on page 4, line 13, with the following amended paragraph:

In particular, it is an object of the invention to provide a generic magnetoresistive 1-transistor-cell semiconductor memory and a fabrication method suitable therefore such that the number of metallization planes and hence the process costs are reduced while at the same time the minimum cell layout of [[6 F_]] $\underline{6F^2}$ which is achieved in the prior art remains the same. In accordance with one fundamental aspect

of the invention, there is provided an integrated magnetoresistive semiconductor memory in which all of the connecting conductors are situated only in two metallization planes and in the polysilicon plane.

Please replace the paragraph beginning on page 4, line 24, with the following amended paragraph:

With the foregoing and other objects in view there is provided, in accordance with the invention, an integrated magnetoresistive semiconductor memory that includes a plurality of memory cells. Each one of the plurality of the memory cells includes a thin tunnel barrier, two magnetic layers isolated by the tunnel barrier, and an activatable isolating element ~~selected from the group~~ consisting of a switching transistor ~~and a diode~~. The memory has integrated connecting conductors including word lines, digit lines, bit lines and at least one line for activating the activatable isolating element of at least one of the plurality of the memory cells. The memory has two metallization planes and a polysilicon connection plane. Each one of the connecting conductors is located in one of the two metallization planes or in the polysilicon connection plane.

Please replace the paragraph beginning on page 5, line 22, with the following amended paragraph:

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for fabricating an integrated magnetoresistive semiconductor memory, that includes steps of: providing an integrated magnetoresistive semiconductor memory including a plurality of memory cells; for each one of the memory cells, providing two magnetic layers that are isolated by a thin tunnel barrier; for each one of the memory cells, providing an activatable isolating element ~~selected from the group~~ consisting of a switching transistor ~~and a diode~~; providing the integrated magnetoresistive semiconductor memory with integrated connecting conductors including word lines, digit lines, bit lines and lines for activating the activatable isolating element of each one of the plurality of the memory cells; providing each one of the connecting conductors in a plane selected from the group consisting of two metallization planes and a polysilicon connection plane; providing the digit lines in a given one of the metallization planes; providing first lines in the given one of the metallization planes and in the polysilicon connection plane; and using the first lines, which have not yet been used in a layout of the

magnetoresistive semiconductor memory, for connecting other elements of the magnetoresistive semiconductor memory.

Please replace the paragraph beginning on page 7, line 20, with the following amended paragraph:

In accordance with what has been said above, the inventive 1-transistor MRAM architecture can be fabricated using only a few process steps on account of the fact that it uses only two metallization planes and the polysilicon connection plane GC, and it thus helps to reduce process costs. In addition, the minimum cell layout of [[6 F_]] $\underline{6F^2}$ can also be retained.

Please replace the paragraph beginning on page 9, line 14, with the following amended paragraph:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 3A thereof, there is shown a planar plan view of a first exemplary embodiment of an inventive magnetoresistive 1-transistor semiconductor memory configuration. Fig. 3B shows a circuit diagram of the first exemplary embodiment of the inventive magnetoresistive 1-transistor semiconductor memory configuration. Both the digit line (DL) 3 and the low-resistance word line connections 10 are situated in the metallization plane M1, while the bit

lines (BL) 5 are situated in the metallization plane M2. The polysilicon word lines 1 are situated in the polysilicon connection plane GC. In this way, the lines 10 in the metallization plane M1 which are not used in the layout (special purpose line) can be used for quickly activating the word lines by supplying a signal via the lines 10. This can be seen from the circuit diagram shown in Fig. 3B. Alternatively, unused lines situated in the polysilicon connection plane GC may also be used for the same purpose. The minimally attainable cell layout of [[6 F_]] $\underline{6F^2}$ is preserved, as indicated by the hatched area 8 in Fig. 3A.

Please add the following new paragraph after the paragraph ending on page 10, line 7:

The circuit diagram depicted in Fig. 3B shows the circuit connections of two exemplary digit lines (DL_0, DL_1)3 with two exemplary bit lines (BL_0, BL_1)5 via respective magnetoresistive memory cells 11, 12, 13 selected by switching transistors 15 which are activatable by signals on word lines 1. The signals on the respective word line 1 are driven by a respective driver A, B upon activation by supplying a signal via line 10, mentioned above as a low-resistance word line connection (Fig. 3A) and situated in the

metallization plane M_1, or alternatively in the polysilicon connection plane GC.

Please replace the paragraph beginning on page 10, line 9, with the following amended paragraph:

Fig. 4 shows a second exemplary embodiment of an inventive integrated magnetoresistive semiconductor memory configuration in which an unused track situated in the M1 metallization plane is used for voltage supply or a track in the polysilicon connection plane GC is used for shorting the transistor 15 to the substrate. It is to be noted that in Fig. 4 the same elements as in Fig. 3B are designated by the same reference signs.